What Is Claimed Is:

1. A processor unit having at least two execution units, switchover means being included, by the use of which one may switch over between at least two operating modes of the processor unit,
wherein the switchover means are designed so that a change from a first operating mode to a second operating mode is triggered by the processor unit accessing a predefined memory address.

2. The processor unit as recited in Claim 1,
wherein the first operating mode corresponds to a safety mode in which the two execution units process equal programs, and means of comparison are provided which compare the statuses of the execution units, created during the processing of the equal programs, for agreement.

3. The processor unit as recited in Claim 2,
wherein the execution units are designed in such a way that they synchronously process the same programs in the first operating mode.

4. The processor unit as recited in Claim 1,
having at least three separate memory regions, in a first operating mode, each execution unit being connected respectively to a first memory region assigned to each execution unit.

5. The processor unit as recited in Claim 1,
having at least two separate memory regions, in the second operating mode, both execution units being connected only to one second memory region assigned to both execution units.

6. The processor unit as recited in Claims 1 and 5, wherein the predefined memory address to which access is to be made is located in the second memory region.

7. The processor unit as recited in Claim 1, having at least two separate memory regions, in the first operating mode, both execution units being connected only to one first memory region assigned to both execution units.

8. The processor unit as recited in Claims 1 and 7, wherein the predefined memory address is included as trigger address in the first memory region, and the following address, to which access is to be made, is included in the second memory region.

9. The processor unit as recited in Claims 1 and 5, wherein monitoring means, especially the switchover means are provided which are designed for monitoring in such a way that the evaluation means are connected in the second operating mode only to the second memory region.

10. The processor unit as recited in Claims 1 and 4, wherein monitoring means, especially the switchover means are provided which are designed for monitoring in such a way that the evaluation means are connected in the first operating mode only respectively to the first memory region.

11. The processor unit as recited in Claims 4 or 5, wherein each of the memory regions is provided in a separate memory module.

12. The processor unit as recited in Claim 2, wherein the means of comparison are switched off in response to the transition into the second operating mode, which is equivalent to a performance mode, and a

comparison of the statuses takes place only in the first operating mode.

13. The processor unit as recited in Claim 1, wherein means of interruption are included which are designed in such a way that they make possible a return to the first operating mode by an interrupt.

14. The processor unit as recited in Claim 13, wherein the interrupt is triggered by a time condition.

15. The processor unit as recited in Claim 13, wherein the interrupt is triggered by a status condition.

16. A method for switching over between at least two operating modes of a processor unit, having at least two execution units, wherein a change from a first operating mode to a second operating mode is triggered by the processor unit accessing a predefined memory address.

17. The method as recited in Claim 16, wherein in the first operating mode, the execution units synchronously process the same programs.

18. The method as recited in Claim 16, wherein in the two operating modes different programs are processed, in the first operating mode, safety-critical programs being redundantly processed by both execution units, and in the second operating mode, non-safety-critical programs being processed.

19. The method as recited in Claim 18, wherein the safety-critical programs are stored redundantly in the first memory regions respectively assigned to the execution units.

20. The method as recited in Claim 18, wherein the non-safety-critical programs are stored in a single second memory region, and both execution units in the second operating mode only access the second memory region.

21. The method as recited in Claim 16, wherein in the first operating mode, safety-critical programs are redundantly processed, and the statuses created in this context are compared for agreement.

22. The method as recited in Claim 16, wherein in the first operating mode, the execution units respectively only access a first memory region assigned to each execution unit.

23. The method as recited in Claim 16, having at least two separate memory regions, in the first operating mode, both execution units accessing only a first memory region assigned to both execution units.

24. The method as recited in Claims 16 and 23, wherein the predefined memory address is included as trigger address in the first memory region, and the following address, to which access is to be made, is included in the second memory region.

25. The method as recited in Claim 16, wherein in the second operating mode, the two execution units only access a second memory region assigned to both execution units.

26. The method as recited in Claims 16 and 25, wherein it is monitored that the evaluation means only access the second memory region in the second operating mode.

27. The method as recited in Claim 16 and 22 or 23, wherein it is monitored that the evaluation means only access the first memory region in the first operating mode.

28. The method as recited in Claim 16, wherein a switchover of the second operating mode to the first operating mode takes place by an interrupt, the interrupt being triggered by a time condition or a status condition.